CLAIMS

1. An integrated circuit, comprising;

a first transistor (P2), comprising:

a first gate region (108) comprised of a semiconductor structure (100) on a substrate; and

a first body region comprised of a semiconductor layer (104), having a first channel region (112) disposed on the first gate region and a source (110) and drain (114) formed on either side of the first channel region;

and

a second transistor (N3) coupled to the first transistor, comprising:

a second body region comprised of the semiconductor structure (102), having a second channel region (118) and a source (116) and drain (120) formed on either side of the second channel region; and

a second gate region (122) comprised of the semiconductor layer (104), disposed on the second channel region.

2. The integrated circuit of claim 1, wherein the semiconductor structure (100, 102) comprises a silicon fin.

3. The integrated circuit of claim 2, wherein the first transistor (P2) comprises an inverted FinFET transistor, and wherein the second transistor (N3) comprises a FinFET transistor.

4. The integrated circuit of claim 1, wherein the drain (114) of the first transistor (P2) is connected to the gate (122) of the second transistor (N3) by the semiconductor layer (104).

5. The integrated circuit of claim 1, further comprising a third transistor (N1), wherein the third transistor comprises:

a third body region comprised of the semiconductor structure (100), having a

third channel region (126) and a source (128) and drain (124) formed on either side of the third channel region; and

a third gate region (129) comprised of the semiconductor layer (106), disposed on the third channel region.

6. The integrated circuit of claim 5, wherein the gate (108) of the first transistor (P2) is connected to the drain (124) of the third transistor (N1) by the semiconductor structure (100).

7. The integrated circuit of claim 5, wherein the first transistor (P2) comprises an inverted FinFET transistor, and wherein the second and third transistors (N3, N1) comprise a FinFET transistor.

8. The integrated circuit of claim 1, further comprising an underpass (80), wherein the underpass allows a portion of the semiconductor structure (82) having a first doping type to insulatively pass under a portion of the semiconductor layer (86) having the first doping type.

9. The integrated circuit of claim 1, wherein the first transistor (P2) comprises a pull-up transistor of a SRAM cell (130), and wherein the second transistor (N3) comprises a pull-down transistor of the SRAM cell.

10. An integrated circuit, comprising:

first and second transistors (P2, N3); and

a single semiconductor layer (104) that forms a source (110), drain (114), and channel (112) of the first transistor and a gate (122) of the second transistor.

11. The integrated circuit according to claim 10, wherein the drain (114) of the first transistor (P2) is connected to the gate (122) of the second transistor (N3).

12. The integrated circuit according to claim 10, further comprising a third transistor (N1), wherein a single semiconductor structure (100) forms a gate (108) of the first transistor (P2) and a source (128), drain (124), and channel (126) of the third transistor.

13. The integrated circuit according to claim 12, wherein the gate (108) of the first transistor (P2) is connected to the drain (124) of the third transistor (N1).

14. The integrated circuit of claim 10, wherein the first transistor (P2) comprises an inverted FinFET transistor, and wherein the second transistor (N3) comprises a FinFET transistor.

15. The integrated circuit of claim 14, wherein the semiconductor layer (104) comprises polysilicon.

16. The integrated circuit of claim 10, wherein the first transistor (P2) comprises a pull-up transistor of a SRAM cell (130), and wherein the second transistor (N3) comprises a pull-down transistor of the SRAM cell.

17. An integrated circuit, comprising:

a semiconductor fin (100);

an inverted FinFET transistor (P2), wherein the fin forms a gate (108) of the inverted FinFET transistor; and

a first FinFET transistor (N1), wherein the fin forms a source (128), drain (124), and channel (126) of the FinFET transistor and wherein the gate of the inverted FinFET transistor is connected to the drain of the first FinFET transistor.

18. The integrated circuit according to claim 17, further comprising:

a second FinFET transistor (N3); and

a semiconductor layer (104), wherein the semiconductor layer forms a source (110), drain (114), and channel (112) of the inverted FinFET transistor and a gate (122) of the

second FinFET transistor, and wherein the drain of the inverted FinFET transistor is connected to the gate of the second FinFET transistor.

19. The integrated circuit of claim 18, wherein the inverted FinFET transistor (P2) comprises a pull-up transistor of a SRAM cell (130), and wherein the second FinFET transistor (N3) comprises a pull-down transistor of the SRAM cell.

20. A method, comprising;

providing a semiconductor fin (100, 102) on a substrate, wherein a portion of the fin forms a gate region (108) of an inverted FinFET transistor (P2) and a body region of a FinFET transistor (N3);

applying a semiconductor layer (104) over the gate region of the inverted FinFET transistor and the body region of the FinFET transistor, wherein the semiconductor layer forms a source (110), drain (114), and channel (112) of the inverted FinFET transistor and a gate region (122) of the FinFET transistor; and

doping the semiconductor layer with a first dopant type to form the source, drain, and channel of the inverted FinFET transistor and a second dopant type to form the gate region of the FinFET transistor.

21. The method of claim 20, wherein the drain (114) of the inverted FinFET transistor (P2) is connected to the gate (122) of the FinFET transistor (N3).

22. The method of claim 20, wherein the inverted FinFET transistor (P2) comprises a pull-up transistor of a SRAM cell (130), and wherein the second FinFET transistor (N3) comprises a pull-down transistor of the SRAM cell.

23. A six device SRAM cell (130), comprising:

a pair of cross-coupled inverters (92, 94), each inverter including a pull-up inverted FinFET transistor (P1, P2) and a pull-down FinFET transistor (N3, N4); and

a pair of coupling FinFET transistors (N1, N2) for respectively coupling the cross-coupled inverters to a bitline (BL) or a complement of the bitline (BL(BAR)).

24. The SRAM cell according to claim 23, wherein the pull-down inverted FinFET transistors (P1, P2) are p-channel, and wherein the pull-down FinFET transistors and the coupling FinFET transistors (N3, N4) are n-channel.